An Optimization Algorithm for Dimensional Design of Graphene Nano-ribbon Field Effect Transistors for All-Graphene SRAM Chip

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Abstract

This work presents a complete all-graphene SRAM chip design. The SRAM requires analog and digital sub-circuits, each having different design criteria. On the other hand, the electrical parameters of a GNRFET device are strongly related to geometry. In this study, we built a complete graphene-based SRAM chip and then proposed a new approach to optimize the GNRFET's physical design which fulfills SRAM requirements for HOLD, READ, and WRITE operations. The effect of geometric and process parameters such as chirality, channel length, and width are investigated on the characteristics of an SRAM cell based on GNRFET. Analysis of power consumption, delay, and SNM results, indicate that adjustable parameters of GNRFETs can have significant effects on SRAM cell performance, and our approach is very effective in parameter optimization. Using optimized GNRFETs, a full-circuit SRAM chip is designed and analyzed. The noise margin test of the SRAM cell shows 188mV HSNM, and 240mV WSNM, while standby and leakage currents were 5, and 20 times smaller.

Keywords: Optimization, Graphene, GNRFET, 6T-SRAM, Sense-Amplifier, Line Edge Roughness

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Introduction

Due to the high demand for more functions and integration, moving toward the smaller dimension is inevitable, however, according to IRDS [1] and ITRS [2], silicon devices are more under question and facing physical constraints on scaling. It could mean in the silicon-dominated microelectronic industry, Moore's Law is nearing its end. To face these fundamental limitations and continue the scaling in the nanometer regime, several research fields are active. The IRDS has provided promising device solutions based on new technologies and new materials, such as graphene, germanene, silicene, or type III-V composite semiconductor materials. However, among the alternative materials, graphene has shown promising results and has been one of the main subjects of interest [1-2].

Graphene is a two-dimensional material in the form of a honeycomb lattice made of carbon atoms, in which the mobility of carriers is far greater than that of silicon and other semiconductor materials [3]. On the other hand, graphene has zero band gap. Even though the zero band gap makes it a strong conductor, however, when is used as a semiconductor, i.e. channel material in a transistor, it makes the device unable to switch off. Different approaches have been proposed to address this problem and add bandgap, including rolling [4], constraints in one dimension, and nano-ribbons [5].

Carbon nanotubes created by rolling graphene ribbons showed unique electrical, physical, and mechanical properties. However, it has serious fabrication problems. Instead, graphene nanoribbons (GNRs) which are created from one-dimensional graphene sheets have a simpler manufacturing process [5]. Due to the atomic thickness and nanometer geometry, GNRFET-based circuits have a higher performance and lower power consumption than CMOS-based circuits [11]. The GNR-based transistors face challenges, such as small band gaps, reduced mobility, and process variations [6-10]. The graphene nanoribbon channel length, width, line edge roughness (LER)[13], doping, and oxide thickness are all among the challenging design parameters of the GNRFET devices, which require different optimization when used for either analog or digital applications[14-16].

Among components, SRAM is a key component in digital design. Millions of SRAM bits are used in digital chips and microprocessors. Toward all-graphene chips, studying reliable SRAM design using GNRFET is crucial. Due to high density, optimum device selection or any possible device level

optimization, can lower the power consumption or reduce the delay of the SRAM cell, which affects the performance on a large scale and enhances circuit reliability.

The SRAM design consists of a cell array, 6T, 8T, and 10T cell forms were introduced. Moving toward all-carbon, the concept is used as a replica for GNRFETs-based SRAM as well. Even though 8T or 10T SRAM cells may show improved power or delay parameters, both require more area and also need more wiring, which is not attractive for building a large SRAM chip. On the other hand, the 6T SRAM cell has a minimum area and standard wiring and routing. A GNRFET 6T SRAM design was introduced in [19] and compared with 45nm silicon, demonstrating cell stability and proving the potential to reduce power consumption. Another study used dual-gate GNRFETs, targeted to lower power and compared to 10nm FinFET [20]. Both works show improved performance but also indicate that GNRFET performance especially the Ion/Ioff parameter is very dependent on the physical device design and arrangement of ribbons[21]. More recent 12T cells will have more power and area issues than earlier [22].

Compared to MOSFET, GNRFETs have more adjustable physical and dimensional parameters. Some parameters have a direct effect on the device and circuit performance, and some have an oscillating feature, so depending on the application, those parameters should optimized and be chosen carefully. On the other hand, the complete SRAM chip design imposes a different requirement to guarantee safe and reliable READ and WRITE operation. In this paper, we explore a new method for GNRFET device design targeting digital and SRAM applications. The study is not limited to the SRAM cell but includes a full chip including an array conditioner, analog sense amplifier, and addressing circuits.

This article is organized as follows: in Section 2, we will take a brief look at the structure of the MOS-GNRFET transistor and review its parameters. It also reviews the optimal parameter selection for the 6T-SRAM circuit and takes a look at its important parameters, such as SNM, delay, and power consumption. In most previous studies the focus was only on SRAM cells, but in this study, as explained in Section 3, we present the complete graphene-based SRAM chip, capable of addressing, storing, reading, and writing data. Section 4 presents the simulation and analysis results, and finally, the conclusion of this study is presented.

2 - The GNRFET Optimization

The MOS-GNRFET is composed of parallel graphene nano-ribbons as a channel, Drain, and Source terminal on each side, and a gate on the top of the nano-ribbons. The carbon atoms' placement in the ribbon can lead to a zigzag or armchair arrangement. The zigzag shows metallic behavior, while the armchair can show a band gap if cut to a narrow width. Figure 1 (a) shows a 2D top view of the GNRFET transistor, in (b) a ribbon structure is represented [16].

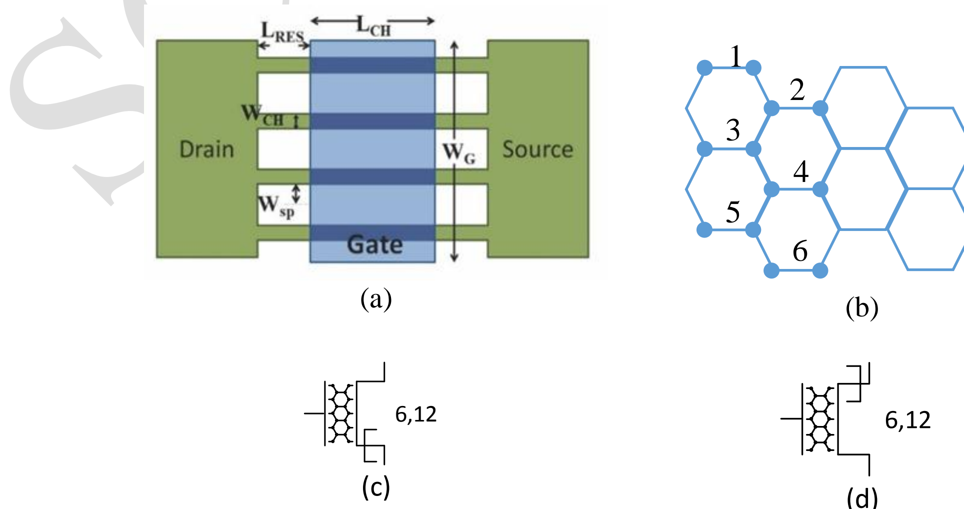

Fig. 1. (a) Top 2D view of the MOS-GNRFET transistor (b) a Nano-Ribbon with N=6 dimmer, (c) symbol for N-type GNRFET, (d) symbol for P-type GNRFET [16]

The GNRs are placed in the channel area with a length of L_{CH}, the width of W_{CH} , and the distance of W_{SP} apart from each other, altogether creating a transistor channel width of W_G. The number of ribbons in GNR is a design parameter and can vary. The spacing between the gate and contacts of GNR is doped with the f_{dop} fraction, which is called a reservoir. The length of the intrinsic part of each ribbon is represented with L_{CH} and the length of the doped part with L_{RES} [5]. Figure 1 (c) and (d) represent the symbols used in this study for N- and P-type GNRFET. Two numbers are shown next to each symbol, the first indicates the number of ribbons and the second specifies the dimmers.

Various models of graphene-based devices have been proposed so far, but only for two models, i.e., MOS-GNRFET and SB-GNRFET, a compact model compatible with SPICE has been introduced. In digital and SRAM applications on and off currents are very important and a higher I_{ON}/I_{OFF} ratio is desired. Among the two types, the MOS-type GNRFET transistor shows a higher I_{ON}/I_{OFF} ratio than the SB type [18]. So, in this study, we used the MOS-GNRFET transistor for the design, analysis, and simulations of the SRAM chip.

In the proposed model, the minimum channel length is 10nm. Also, a maximum channel length of 100 nm has been considered to fulfill the assumption of ballistic transmission. As the channel length decreases, the off-state current of the GNRFET increases which causes a decrease in the I_{ON}/I_{OFF} ratio, and an increase in the DIBL effect. On the other hand, in the short channel, the mean free path of the carriers is shorter than the length of the channel, and hence the transmission will be non-collision and ballistic. These parameters are adjustable in the SPICE model [16].

The amount of impurity in the GNRs will be at least 0.001 and at most 0.015 based on the information in [16]. Part of the GNR that lies just below the gate is intrinsic, and doping is applied to the GNR area that lies below the area between the gate and the contacts. The N-GNRFET is made by placing n-type impurities in the reservoir region, and the P-GNRFET by p-type impurities. These parameters have a major effect on device operation and circuit parameters, so depending on the application requirements, a proper parameter selection or optimization is needed.

3- Design of MOS-GNRFET Based SRAM

The complete SRAM chip needs several blocks to perform basic READ, WRITE, and HOLD operations. Figure 2 shows those needed blocks which were all designed and tested using GNR transistors. The main storage element is the 6T-SRAM cell, used to create a 16x1 array. The READ and WRITE operation requires an address decoder which is composed of digital gates; while analog operation is needed for bit/bit_b lines conditioning and sense amplifier to write and read the stored data.

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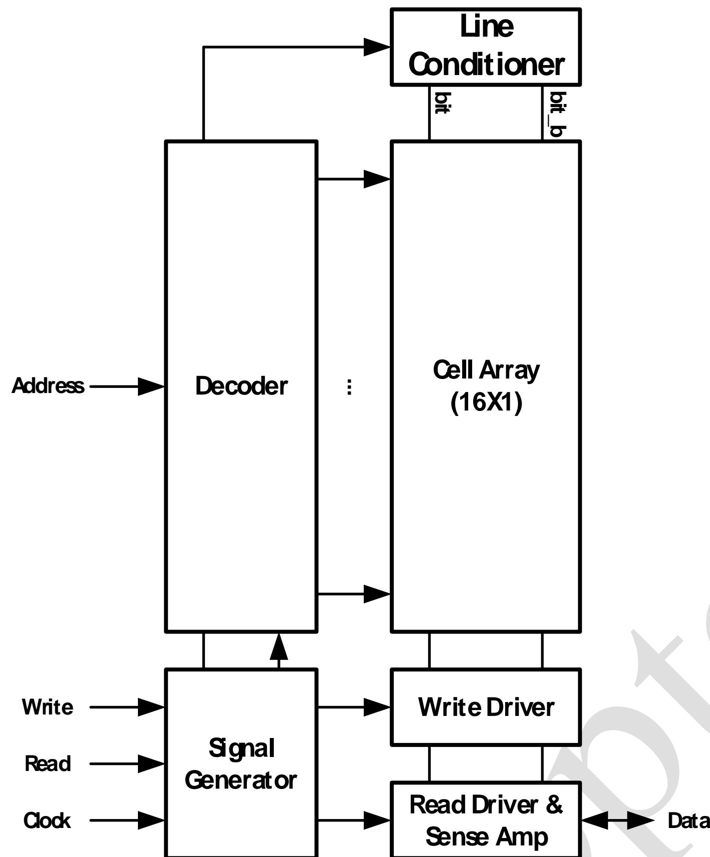
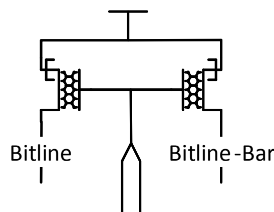


Fig. 2. SRAM building blocks

The Signal Generator block receives Write and Read commands aligned with the Clock and creates the required internal timing and activation signals for the Line Conditioner, Write Driver & Sense Amplifier. The address goes to the decoder to select the targeted cell in the array. Several logic gates are used in the decoder, write driver, and signal generator blocks, since the design process of these graphene-based logic gates is similar to CMOS gates and has already been studied and investigated, we used available approaches [19-21] and focused on SRAM cell design. So, the following is the new approach and steps taken to design the required analog blocks, and optimize the 6T storage cell, to design the SRAM chip.

Among those required analog blocks is the line conditioner, shown in Fig 3. When the signal generator detects a WRITE or READ operation, it asserts a Conditioning signal to turn pull-up P-GNRFETs on, which charges up the Bitline and Bitline-Bar lines to the VDD level. In the next step,



depending on the operation, the charge is processed by the sense amplifier or write driver.

Fig. 3. bit and bi_b line conditioner circuit

The next essential analog circuit is the Sense Amplifier for the read circuit, which is shown in Fig. 4 and consists of a graphene-based differential pair followed by graphene-based logic gates to read the stored value. In the READ mode, the conditioner circuit of Fig. 3 will charge both Bitline and Bitline-Bar line up to VDD, but after accessing the targeted cell and depending on stored data there will be a charge difference. The differential pair which is active in the READ mode, senses the imbalance

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between those lines, and after amplification and filtering, the output will change according to the cell's stored value.

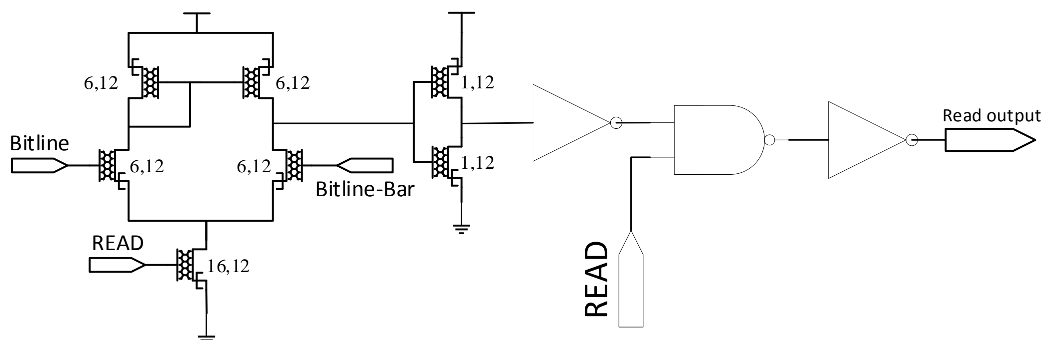

Fig. 4. Sense Amplifier and Read circuit

The main storage element of the SRAM chip in Fig. 1 is the 6T cell. In our approach, we first design and simulate each block, then build the simulation model of the SRAM chip. With complete simulation mode, cell optimization is done using HSPICE and MATLAB codes. The HSPICE simulation tool is used with a 0.5V circuit supply at room temperature. For devices, the MOS-Type [16] GNRFET transistor model is used, which has an adjustable range of geometric and process parameters. As a sample of simulations, Bitline and Bitline-Bar, and conditioner circuit operation are shown in Fig 5. In this figure up to 1.5ns circuit is in the write mode and bit/bit_b lines are charged in opposite directions, while after switching to read mode, those lines are charged similarly, which is essential for SRAM operation.

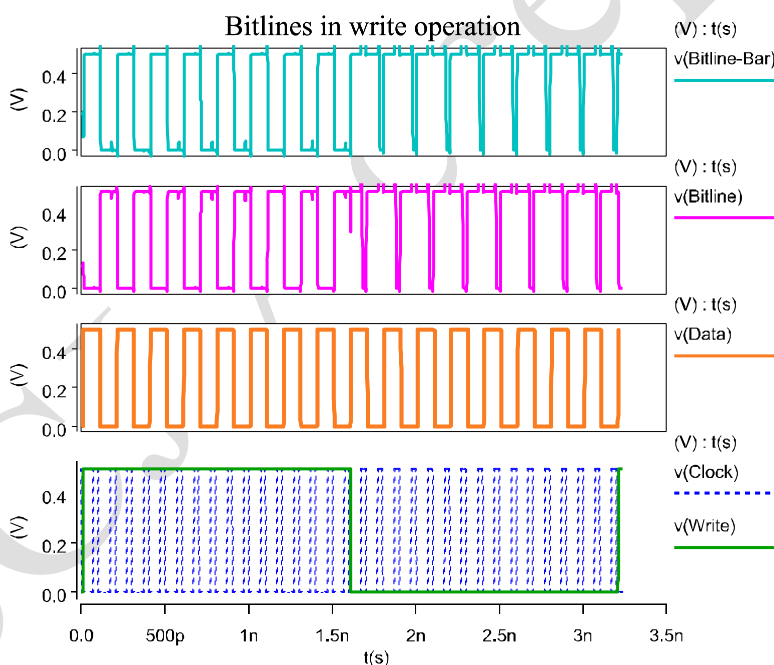

Fig. 5. bit and bit_b line conditioner in the read and write mode.

After building and simulating all needed blocks, we switched to the design and optimization of the SRAM cell. Using a 6T SRAM cell as shown in Fig. 6, which has a pull-up, pull-down, and access GNRFETs. The cell should be able to keep the data, but it also needs to be writable and non-destructive when a read is performed. It also should show good noise margins along with low power consumption in all modes. These requirements and the success of the cell operation are very dependent on the proper selection and sizing of the ribbon and dimer for each GNRFET.

We developed a code and optimization algorithm, which integrates MATLAB and HSPICE. The algorithm starts in MATLAB by creating a candidate group of possible 6T SRAM cell circuits. To create this group, we observe the criteria mentioned in Table 1 for pull-up, pull-down, and access GNRFETs, the initial population of this group is 500 circuits.

Table 1. Parameter range to create an initial population

Transistors	Number of Ribbon (N_{Rib})	Number of Dimmer (N)
Pull up (MPU, MPUL)	1	6-12
Access (MAC, MACL)	1-3	6-12
Pull down (MPD, MPDL)	1-6	6-12

After generating candidate cell circuits, the algorithm uses HSPICE for circuit simulation and performs a write test. Figure 6 shows the test circuit condition during the write operation. For each cell, this test is done under different logic values and in the 200ps transient time, then rise and fall times along with leakage current are recorded.

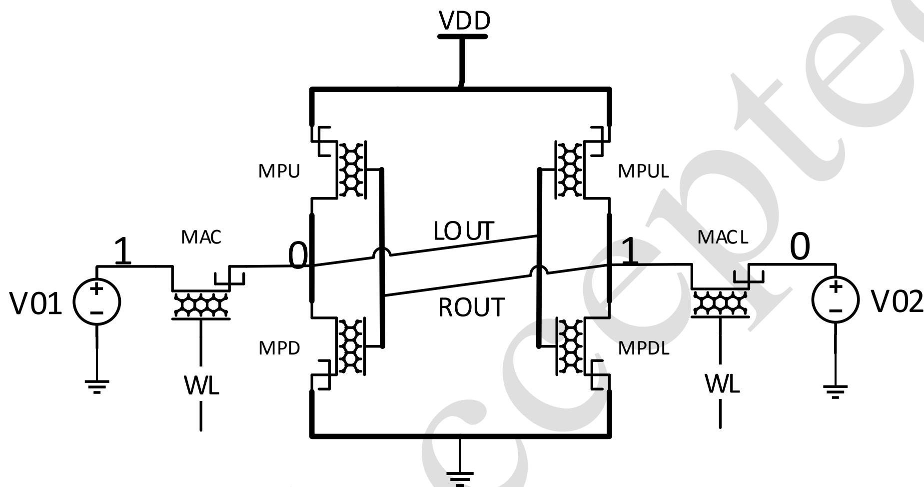

Fig. 6. 6T cell circuit for the write operation.

The simulation results are read back to MATLAB to check if a write operation was successful on each cell or failed. After eliminating failed cells, in the second step, the remaining cells go to the reading test. The READ operation on 6T SRAM is sensitive, and in the case of improper transistor sizing, the operation can be destructive and data will be lost. Figure 7 shows the circuit for the reading test of each cell. To simulate actual conditions and keep modeling accuracy, two pre-charged capacitors are added to the access lines, and read simulation is done in 200 ps transient duration. Those capacitors help to emulate the bit/bit_b lines charge effect and put the cell under full stress. During these read simulations, circuit timing parameters and leakage are recorded to see if stored data in the cell is flipping or cell withstand the stress and can keep the data.

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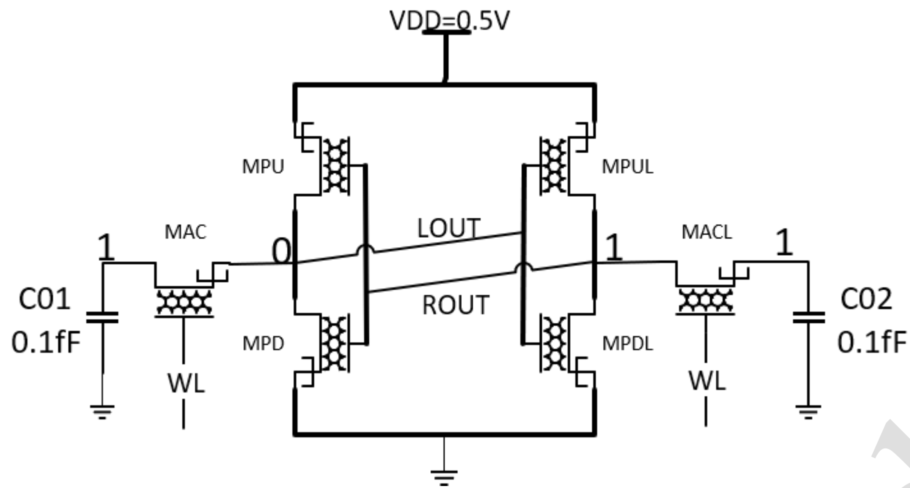

Fig. 7. 6T cell for a read operation test.

By analyzing the simulation results in MATLAB, a cell is kept for the next step if the read was successful, otherwise removed from the search group. In the third step, static-noise margins or SNM simulation is carried out and margins are measured. Figure 8 shows the SNM and leakage current scattering plot.

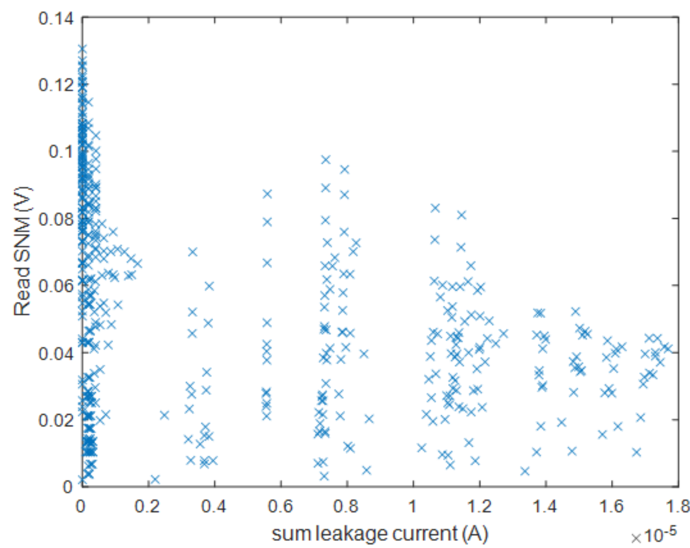

Fig. 8. Leakage current and SNM scattering of analyzed cells

So far, all circuits remaining in the optimization process are capable of READ and WRITE operation but have different leakage currents and power consumption parameters. After sorting results based on leakage current and SNM, 34 circuits had better performance compared to [20]. Among those better circuits, the algorithm selects a circuit that has minimum leakage current. Figure 9 shows the 6T-SRAM with the selected GNRFET sizing.

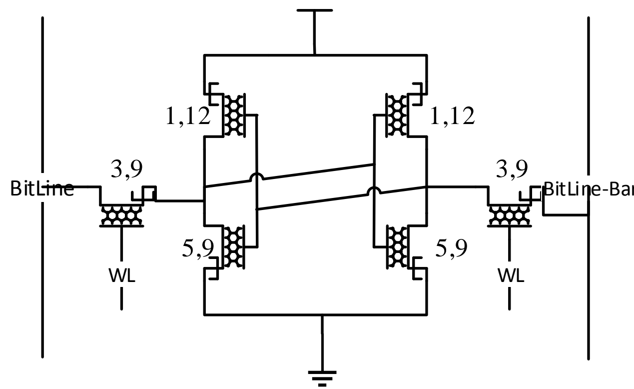

Fig. 9. Selected cell after optimization

After selecting the best cell, a memory array of 16x1 is created, and a decoder circuit along with Bitline and Bitline-Bar conditioning and the sense amplifier is added to complete a graphene-based SRAM chip. Using external access pins, write and read operations are carried out on the chip. The static noise margin metrics in the hold, read, and write modes are deployed to compare and characterize the design [21][22]. In the hold mode, the cell is isolated from access and decoder circuits and checked for stability measures. Figure 10 shows the butterfly representation of SNM in the hold mode or HSNM. The measured symmetric SNM in this mode is 188mV which is 6mV higher than the competing design [20].

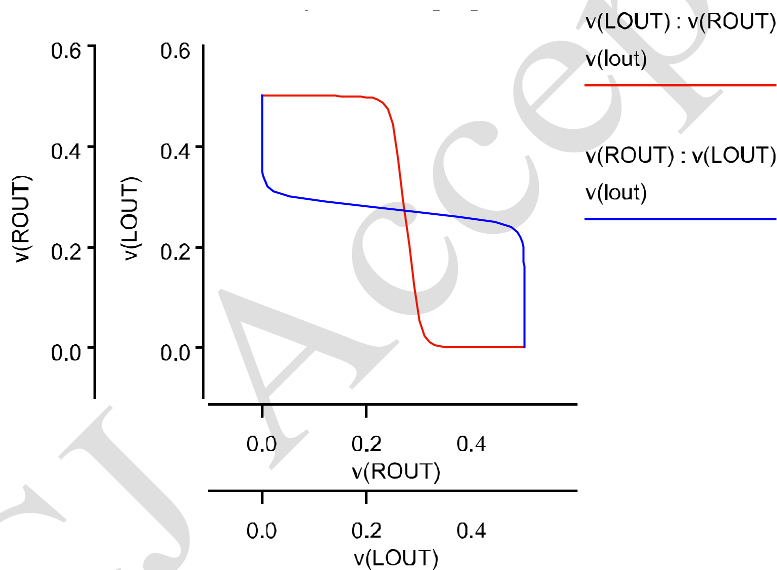

Fig. 10. HSNM measurements, in reading mode.

The SNM in write mode indicates the capability of the cell to be written easily. The measured SNM in write mode shown in the Fig. 11, is 240mV which is 46mV wider with respect to competing designs [20].

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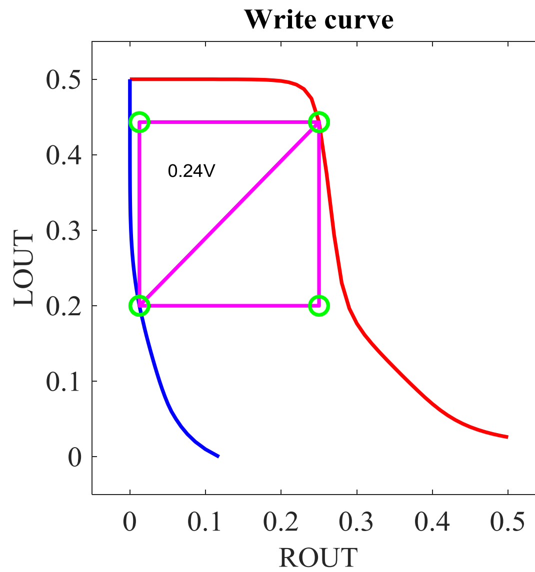

Fig. 11. Measured write mode SNM

The SNM in read mode indicates how a cell is read while the operation is not destructive and can hold the data. The measured read SNM shown in Fig. 12, is 106mV which is 2mV wider than previous work [20].

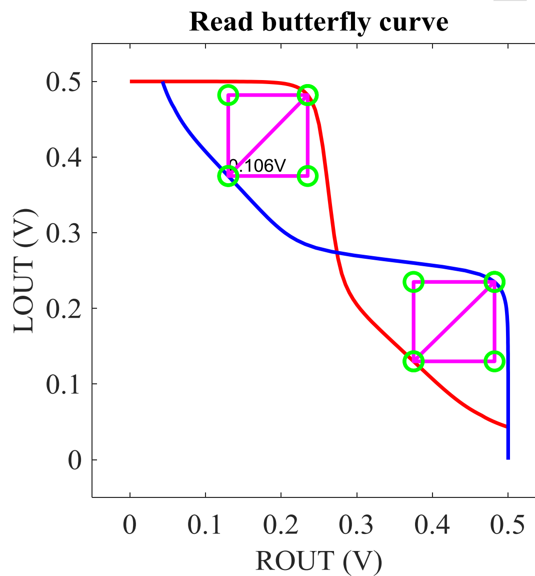

Fig. 12. Measured SNM in the read mode

To have an insight for possible future fabrication a layout design is suggested. Using available layout design tools and mimicking the graphene layer, the approximate layout of the SRAM cell is shown in Fig. 13, the estimated cell area is $2355nm^2$.

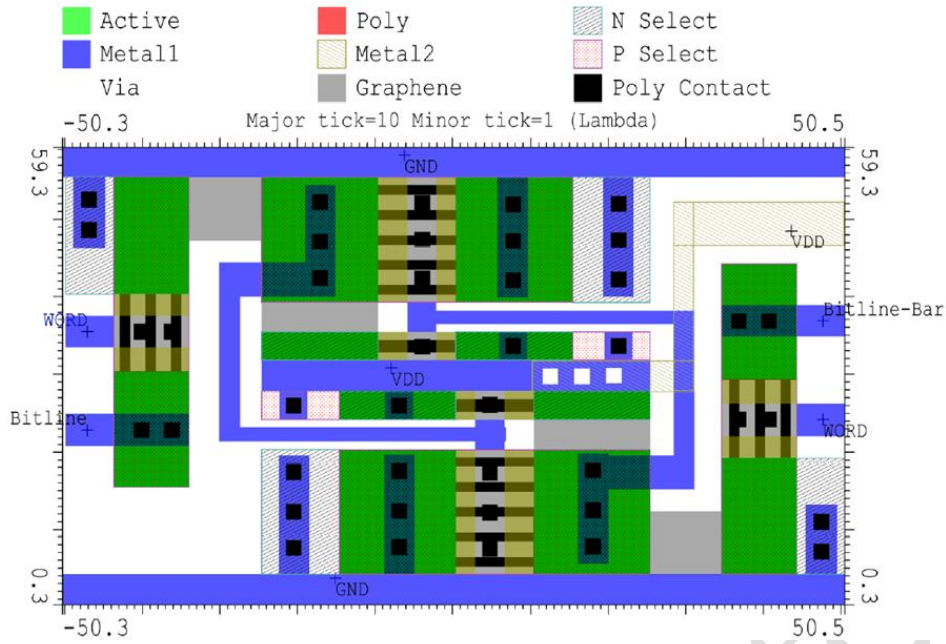

Fig. 13. Proposed layout of 6T GNRFET SRAM cell

Table 2 shows the test and simulation results comparison of the proposed circuit with respect to the competing work [20]. In this table, it would be helpful to consider that each GNRFET needs two-dimensional parameters, and there are three sets of FETs in the 6T SRAM cell. At the same technology and supply voltage, the WSNM and WTV are improved, even if we consider SNMs in the similar range, the main improvement is in the standby and leakage current, which are 5 times and 20 times smaller, respectively. We would like to mention that the subject of our study is not limited to the SRAM cell itself, but include all necessary blocks to build an all-graphene SRAM chip. This study along with the IO design [23] are steps toward a complete all-graphene SRAM design.

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Table 2: Simulation and comparison results for SRAM cell

Design		SRAM-G(*)	[٢٠] SRAM-G
Technology		nm١٠	
Supply Voltage		mV٥٠٠	
PU-AC-PD	nRib	١_٣_٥	١_٢_٥
	N	١٢_٩_٩	١٢_١٢_١٢
(Standby Current (pA		١٦٤	٨٣٦
(Leakage Current (pA		١٣,٦٧	٢٦٦,٧
Read	(Current (nA	٠,٦٨٩	١,٠١٩
	(Delay (pS	٨,٤٣٣	٦,٨٢٢
Write	(Current (nA	٢٢٦,٣٨	١٧٢,٠٥
	(Delay (pS	٤,٢	٤
(HSNM (mV		١٨٨	١٨٢
(RSNM (mV		١٠٥,٧	١٠٣,٧
(WSNM (mV		٢٤٠	١٩٤
(SVNM (mV		٢٤١,٩٦	٢٣٩,١١

(SINM (μA	٨,٧٦٥	١٥,٨٨
(WTV (mV	٢١٤,٤٣	١٩٢,٥٢
(WTI (μA	١,٨٣٧-	٤,٦٢-
٢(Approximate Cell Area (nm	٢٣٥٤,٩	٢٣٠٣,٢

Conclusion

In this paper, we investigate a new design and optimization algorithm targeted to all-graphene SRAM chips. The aim was to design all the parts needed for an SRAM chip, including digital and analog sections. The base storage cell was 6T SRAM designed using GNRFETs, in which transistor proper sizing was done in three steps using an optimization algorithm. The initial population for SRAM cells was created in MATLAB, after HSPICE time domain simulation, the read-and-write test and related measurements were done. Then operational best cells were subject to the SNM test. The final set of successful cells is sorted according to their leakage current and power consumption, then the best cell and transistor sizing is selected. Using the selected best cell, an array is created and a necessary circuit for address decoding is added, then conditioning and the sense amplifier is added to make a complete SRAM chip, all designed using MOS-GNRFET. The complete SRAM chip then went to more testing and characterization. The butterfly noise test of the SRAM cell showed 188mV HSNM, and 240mV WSNM, while standby and leakage currents were 5, and 20 times lower than the competing design.

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